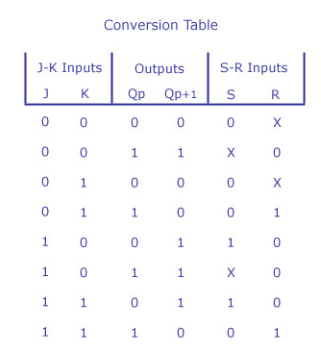
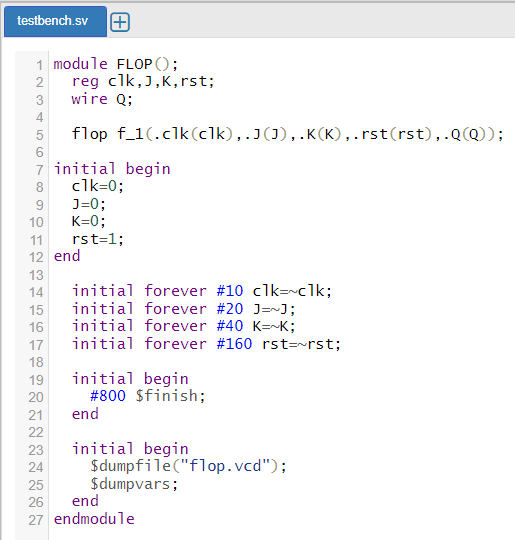
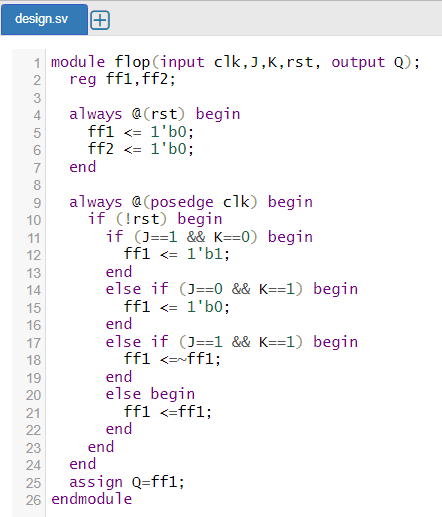
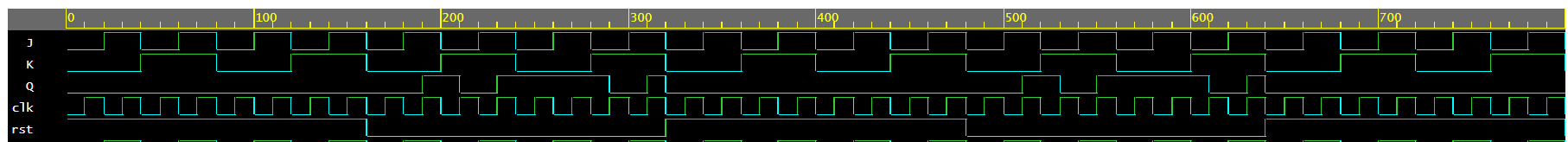
**Lab 10: Flip Flops Conversion**

**Question 1: Modify the S-R flip flop created in last lab into JK flip flop. Verify the functionality of J-K flip flop using suitable Testbench.**

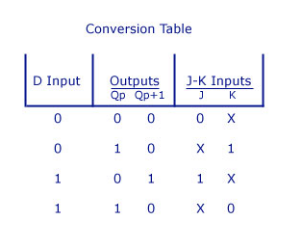


**Conversion Expression:** S = J’Q and R = KQ

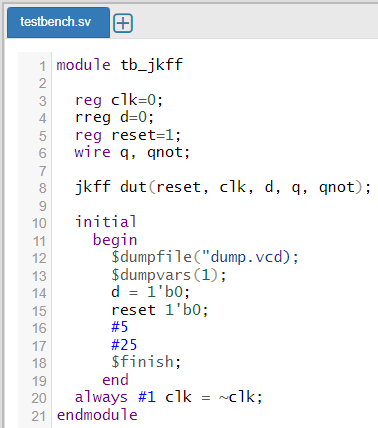
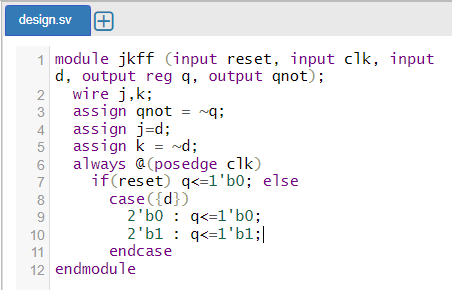
** **

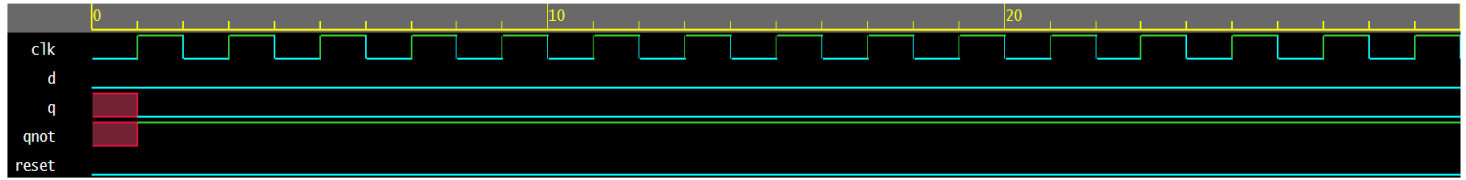
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**Question 2: Develop the behavioural Verilog module of D flip-flop, converting it from a J-K flip flop. You may utilize if-else statements to develop your Verilog code. Verify the functionality via a suitable test bench code.**

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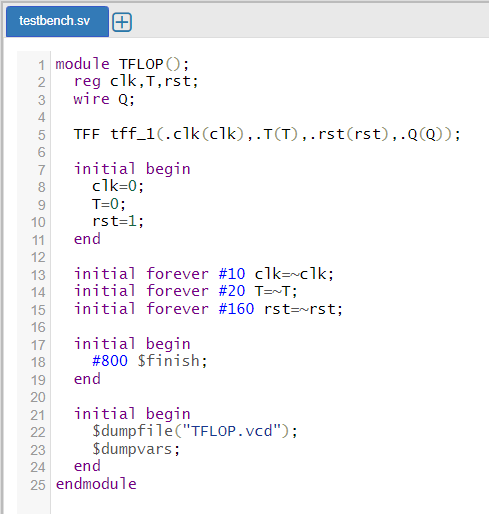
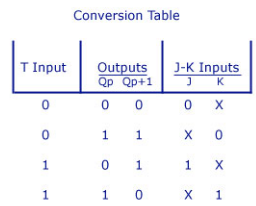
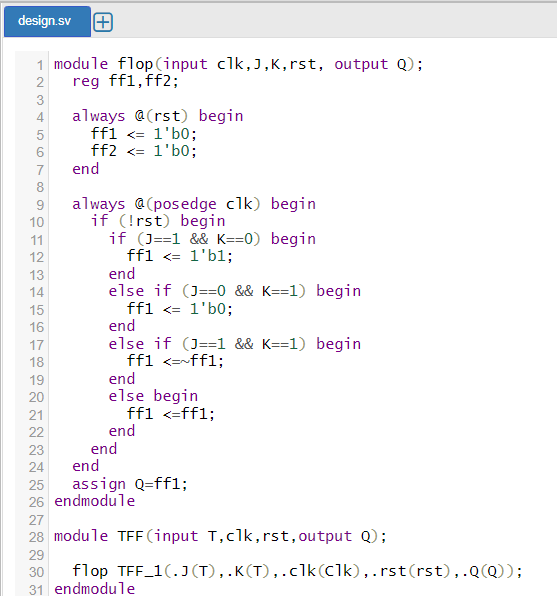
**Conversion Expression:** J = D and K = D’

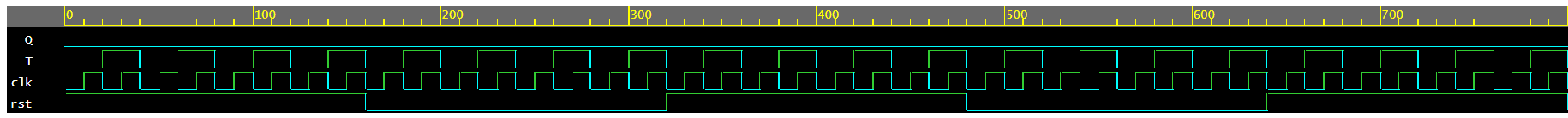
** **

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**Question 3: Develop a behavioural Verilog module for JK flip flop using case statements. Modify it to act like a T flip flop. Validate the modification via a suitable test bench.**

**Conversion Expression:** J = T and K = T

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